AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-21. (Canceled)

22. (Previously Presented) An apparatus, comprising:

a communication path to exchange information packets;

a processor to process information packets;

a buffer pool register cache local to the processor to store free buffer handles for information packets if the buffer pool cache is not full, wherein the buffer pool register cache is to store buffer handles associated with both receive and transmit operations; and

a non-local memory to store free buffer handles for information packets if the buffer pool register cache local to the processor is full, wherein the non-local memory is not accessed if the buffer pool register cache local to the processor is not full.

23. (New) The apparatus of claim 22, wherein the processor is associated with a network processor.

24. (New) The apparatus of claim 23, wherein the processor is a receive processor of the network processor.

25. (New) The apparatus of claim 23, wherein the processor is a transmit processor of the network processor.

26. (New) The apparatus of claim 23, wherein the network processor includes:

a control plane processor.

27. (New) The apparatus of claim 22, wherein the communication path comprises:

an input path for receiving information packets; and

an output path for transmitting information packets.

28. (New) The apparatus of claim 22, wherein the communication path comprises:

a memory path for fetching and freeing buffers.

29. (New) The apparatus of claim 22, wherein the communication path connects to at least one of a dynamic random access memory or a static random access memory.

30. (New) The apparatus of claim 22, wherein the buffer pool register cache is a set of next neighbor registers configured to form a next neighbor ring.

31. (New) The apparatus of claim 22, further comprising:

a communication interface device coupled to the communication path.